CLAIMS:

1. A method of transmitting information between an information transmitter and an information receiver, the potential difference of which moves in cycles between a minimum value and a maximum value and is situated at the minimum value for regular intervals; having the steps:

- provision of information about the time interval or determination of the time interval in which the potential difference between information transmitter and information receiver reaches its minimum value;

- closing of a switching means of the information transmitter to an information memory assigned to the information receiver, only within the time interval; and

- transmission and storage of the information in the information memory.

2. A method as claimed in claim 1, characterized in that the information is stored in the information memory as a set of charges.

3. A method as claimed in claim 1 or 2, characterized in that the information is a current value which is supplied over a predetermined on-time of the switching means.

4. A method as claimed in claim 1 or 2, characterized in that the information is a voltage value.

5. A method as claimed in claim 1 or 2, characterized in that the information is a time value.

6. A method as claimed in claim 4, characterized in that the voltage value is used to set, synchronize or trace the frequency of a voltage-controlled oscillator, which then triggers events by way of counter registers.

7. A method as claimed in claim 5, carried out in a driver circuit for controlling upper switching means as information receiver and lower switching means, where the control

electronics, which are at the potential of the lower switching means, form the information transmitter, for converting a DC voltage into a clocked output voltage which has a high-voltage part for controlling the upper switching means and a low-voltage part for controlling the lower switching means, characterized in that the current value (I_1) for generating the set of charges is made to be proportional to the discharge current (I_2), so that

$$I_1 = k * I_2 \text{ with } k > r_{max} > 1,$$

where r_{max} is the maximum occurring duty cycle, defined as the maximum on-time of the upper switching means divided by the minimum on-time of the lower switching means.

8. A method as claimed in one of claims 1 to 4, carried out in a driver circuit for controlling upper switching means as information receiver and lower switching means, where the control electronics, which are at the potential of the lower switching means, form the information transmitter, for converting a DC voltage into a clocked output voltage which has a high-voltage part for controlling the upper switching means and a low-voltage part for controlling the lower switching means, characterized in that

- a current value is determined which corresponds to a switch-off condition of the upper switching means, and
- the information memory is charged to a voltage that is proportional to the current value of the switch-off condition.

9. A method as claimed in one of claims 1 to 4, carried out in a driver circuit for controlling upper switching means as information receiver and lower switching means, where the control electronics, which are at the potential of the lower switching means, form the information transmitter, for converting a DC voltage into a clocked output voltage which has a high-voltage part for controlling the upper switching means and a low-voltage part for controlling the lower switching means, characterized in that

- a current value is determined which corresponds to a switch-off condition of a load controlled by the driver circuit, and
- the information memory is charged to a voltage that is proportional to the current value of the switch-off condition,

where the switch-off condition is a previously determined excess current across the upper switching means.

10. A method as claimed in claim 1, carried out in a driver circuit for controlling upper switching means as information receiver and lower switching means, where the control electronics, which are at the potential of the lower switching means, form the information transmitter, for converting a DC voltage into a clocked output voltage which has a high-voltage part for controlling the upper switching means and a low-voltage part for controlling the lower switching means, characterized in that

- during the time at the minimum value of the potential difference, the information memory is charged to a voltage that is proportional to the on-time of the upper switching means, and

- after the upper switching means have reached the maximum value of the potential, the voltage is converted back into a time.

11. A driver circuit for controlling upper switching means as information receiver and lower switching means as information transmitter for converting a DC voltage into a clocked output voltage which has a high-voltage part for controlling the upper switching means and a low-voltage part for controlling the lower switching means, characterized in that there is provided

- a device for providing information about the time interval or for determining the time interval in which the potential difference between information transmitter and information receiver reaches its minimum value;

- a switching means which closes a connection from the information transmitter to an information memory for the information which is assigned to the information receiver, only within the time interval.

12. A driver circuit as claimed in claim 11, characterized in that the information memory is an analog memory or a digital memory.

13. A driver circuit as claimed in claim 12, characterized in that the information memory is a capacitor.

14. A driver circuit as claimed in claim 12, characterized in that the information memory is a counter or a register.

15. A driver circuit as claimed in claim 13, characterized in that the current value (I_1) for generating the set of charges in the capacitor is made to be proportional to the discharge current (I_2) of the capacitor, so that

$I_1 = k * I_2$ with $k > r_{max} > 1$,

where r_{max} is the maximum occurring duty cycle, defined as the maximum on-time of the upper switching means divided by the minimum on-time of the lower switching means.

16. A driver circuit as claimed in claim 14, characterized in that the counter counts a first number (N_1) of steps for the upper switching means and a second number (N_2) of steps for the lower switching means, where

$N_1 = k * N_2$ with $k > r_{max} > 1$,

where r_{max} is the maximum occurring duty cycle, defined as the maximum on-time of the upper switching means divided by the minimum on-time of the lower switching means.

17. A driver circuit as claimed in claim 11, characterized in that

- it has a device for determining a current value which corresponds to a switch-off condition of the upper switching means, and in that
- the information memory is charged to a voltage that is proportional to the current value of the switch-off condition.

18. A driver circuit as claimed in claim 11, characterized in that

- it has a device for determining a current value which corresponds to a switch-off condition of a load controlled by the driver circuit, and in that
- the information memory is charged to a voltage that is proportional to the current value of the switch-off condition,

where the switch-off condition is a previously determined excess current across the upper switching means.